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EXAMINER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/647,217	KAYUKAWA ET AL.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) *1-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

1. Applicant's Request for Continued Examination (RCE) and an amendment (including amended claims) filed on 06/19/2007 have been entered.

2. Applicant's arguments filed on 06/19/2007 have been fully considered but they are not persuasive.

3. The applicant contends, "With respect to claim 24, Applicant submits the Hashizume fails to teach or suggest, at least, "...resetting said plurality of flip-flops at a transition time between said test mode and said normal mode responsive to said scan mode signal..." As discussed above, Hashizume only teaches the DC test control circuit 3 set/resets the flip-flops during the TESTMODE_by loading the flip-flops with data from TESTC (Hashizume: column 6, lines 46-51; column 8, lines 32-34). Hashizume does not reset flip-flops BSR0-BSR3, BLU and BLD during the transition time between the test mode and normal mode, and thereby does not prevent the reading of normal mode data until one cycle after issuing the test signal. This one-cycle delay proves that Hashizume does not reset the flip-flops during the transition time between the test mode and normal mode, or the normal mode and test mode."

The examiner disagrees and would like to point out that Hashizume teaches that FIG. 36 illustrates the structure of a main part of a semiconductor integrated circuit device according to a seventeenth embodiment of the present invention. In the structure shown in FIG. 36, two test modes EXTEST1 and EXTEST2 are prepared for a boundary scan test circuit. When an external test instruction EXTEST1 or EXTEST2 is set in an instruction register 41, an instruction decoder 42 supplies a DC test mode control signal DCTM setting all boundary scan registers provided in correspondence to output cells included in a boundary scan register chain (BSR chain) 100 to set or reset states to a BSR control circuit 30 (or 3). BSR control circuit 30 (or 3) drives a set signal Set or a reset signal Reset to an active state in accordance with DC test mode control signal DCTM supplied from instruction decoder 42 and sets the boundary scan registers corresponding to the output cells included in BSR chain 100 to set or reset states.

An external instruction EXTEST, which is generally utilized in a boundary scan test, is an instruction for performing data input/output between the boundary scan registers and a device external to the device

(integrated circuit device). The external test instruction EXTEST is employed in verifying connection between the integrated circuit device (device) and an external logic circuit or testing the external logic circuit. When the external test instruction EXTEST is supplied, a cell connected to an output pin terminal of boundary scan register chain (BSR chain) 100 outputs data (FIG. 36, col. 33, lines 49 to col. 34 line 8, Hashizume).

Hashizume also teaches that when the external test instruction EXTEST1 or EXTEST2 is supplied, instruction decoder 42 supplies a DC test mode control signal DCTM to BSR control circuit 30 (or 3) for setting the boundary scan registers included in BSR chain 100 in set or reset states. Therefore, no time is required for preloading and a shift operation dissimilarly to an ordinary boundary scan test, and the output cell (including an I/O cell) is simply set in a set or reset state, and signals of "1" or "0" can be output from all output terminals by setting the boundary scan registers connected to the output terminals and an output control signal to set/reset states. Thus, the voltage levels of the output signals can be readily measured (col. 34, lines 31-43, Hashizume).

4. The applicant contends, "For similar reasons, Hashizume does not disclose, teach, or suggest at least the features of access control means for prohibiting access to said memory means during said test mode, the prohibiting being switched at a transition time between said test mode and said normal mode in accordance with a mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal, recited in claim 31. In particular, Hashizume does not identify the initiation of a mode change until a clock cycle after the transition. Therefore, Hashizume cannot initiate any action prior to one cycle after the mode transition."

The examiner disagrees and would like to point out that Cavaliere et al. teach memory means connected to the plurality of flip-flops, and access control means for prohibiting access to the memory means during the test mode in accordance with a mode signal (col. 6, lines 6-8, lines 25-29, Cavaliere et al.).

Hashizume teaches a semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising: a plurality of flip-flops arranged so as to perform scan testing for the internal logical circuitry; switching at a transition time between the test mode and the normal mode in accordance with a mode signal; for selectively specifying one of the normal operation

mode and the test mode by the logical level of the mode signal (fig. 1A, 1b, 2, 36, col. 5, line 42 to col. 6, line 14, col. 6, lines 46-51, col. 7, lines 12-25, col. 33, lines 49 to col. 34 line 8, col. 34, lines 31-43, Hashizume).

5. The applicant contends, " Independent claims 34, 36, and 41 also include similar subject matter to claim 24, not found in Hashizume. Furthermore, dependent claims 25-30, 32, 33, 35, 37-40, and 42-44 depend on the independent claims and therefore include the features of the independent claims not found in Hashizume."

The examiner disagrees and would like to point out that independent claims 34, 36, and 41 are also rejected because of the similar reasons for claim 24. Please see the examiner's response to arguments for claim 24 above.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claim 24, 25, 27, 32 rejected under 35 U.S.C. 102(e) as being anticipated by Hashizume (US 6,539,511 B1).

Hashizume anticipates claim 24.

Hashizume teaches a semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising: a scan in terminal providing an inputted scan pattern to a scan chain between said scan in terminal and a scan out terminal; a plurality of flip-flops arranged in said scan chain so as to perform scan testing for said internal logical circuitry responsive to said scan pattern; a scan mode terminal providing a scan mode signal for switching said internal logic circuitry between said normal operation state and a scan operation state including said test mode; and a reset

means for resetting said plurality of flip-flops at a transition time, between said test mode and said normal mode, responsive to said scan mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal (fig. 1A, 1B, 2, 4, 14, 27, 36, col. 5, lines 60-65, col. 6, lines 45-51, lines 56-67, col. 7, lines 39-43, col. 14, line 55 to col. 15, line 6, col. 15, lines 18-23, lines 40-46, col. 23, lines 53-58, col. 24, lines 12-13, col. 33, lines 49 to col. 34 line 8, col. 34, lines 31-43, Hashizume).

- Hashizume anticipates claim 25.

Hashizume teaches the semiconductor integrated circuit, further comprising output control means that is connected serially to said plurality of flip-flops, and which outputs data that is supplied during said test mode while prohibiting the outputting of data that is supplied during said normal operation mode (fig. 2, 4, 14, col. 15, lines 11-20, Hashizume).

- Hashizume anticipates claim 27.

Hashizume teaches that said plurality of flip-flops are serially arranged so as to perform scan testing for said internal logical circuitry (fig. 1A, 1B, 4, col. 5, lines 52-54, col. 6, lines 3-6, Hashizume).

- Hashizume anticipates claim 32.

Hashizume teaches a method of testing a semiconductor integrated circuit as defined in claim 24, wherein said plurality of flip-flops are reset at said transition time, between said test mode and said normal mode (FIG. 36, col. 33, lines 49 to col. 34 line 8, col. 34, lines 31-43, Hashizume).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashizume (US 6,539,511 B1) as applied to claim 25 above, and further in view of Cavaliere et al. (US 3,961,254).

As per claim 26, Hashizume substantially teaches the claimed invention described in claim 25 (as rejected above).

However Hashizume does not explicitly teach the specific use of the semiconductor integrated circuit, further comprising: memory means connected to said plurality of flip-flops; and access control means for prohibiting access to said memory means during said test mode responsive to said mode signal.

Cavaliere et al. in an analogous art teach an LSI semiconductor device comprising a memory array, including address, data and buffer registers (col. 6, lines 6-8, Cavaliere et al.). Cavaliere et al. also teach inhibiting access between the logic circuitry and the memory array when the device is in a test mode (col. 6, lines 26-28, Cavaliere et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hashizume's patent with the teachings of Cavaliere et al. by including an additional step of using the semiconductor integrated circuit, further comprising: memory means connected to said plurality of flip-flops; and access control means for prohibiting access to said memory means during said test mode responsive to said mode signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to prevent access to data stored in the memory during the test mode so that the data is not corrupted.

11. Claims 28, 29, 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashizume (US 6,539,511 B1) as applied to claim 24 above, and further in view of Tamamura et al. (US 6,118,316).

As per claim 28, Hashizume substantially teaches the claimed invention described in claim 24 (as rejected above). Hashizume also teaches that the reset means resets said plurality of flip-flops (col. 6, lines 56-67, col. 7, lines 31-33, Hashizume).

However Hashizume does not explicitly teach the specific use of the transition detection means for detecting the transition time of said logical level of said mode signal.

Tamamura et al. in an analogous art teach that as shown in FIG. 3, the pulse generating circuit 5 detects a transition timing (an edge) of the input data 1b, and generates a detected pulse signal 5a so as to be triggered by the transition timing (fig. 3, col. 1, lines 53-56, Tamamura et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hashizume's patent with the teachings of Tamamura et al. by including an additional step of using the transition detection means for detecting the transition time of said logical level of said mode signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the transition detection means for detecting the transition time of said logical level of said mode signal would provide the opportunity to reset the circuit elements for the new mode of circuit operation.

- As per claim 29, Hashizume and Tamamura et al. teach the additional limitations.

Hashizume teaches that the reset means resets said plurality of flip-flops (fig. 2, 4, col. 6, lines 56-67, col. 7, lines 31-33, Hashizume).

Tamamura et al. teach transition detection means for detecting the transition time of said logical level of said mode signal (fig. 3, col. 1, lines 53-56, Tamamura et al.).

- As per claim 33, Hashizume and Tamamura et al. teach the additional limitations.

Hashizume teaches a method of testing a semiconductor integrated circuit as defined in claim 28, wherein said plurality of flip-flops are reset at said transition time, between said test mode and said normal mode (FIG. 36, col. 33, lines 49 to col. 34 line 8, col. 34, lines 31-43, Hashizume).

12. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashizume (US 6,539,511 B1) in view of Cavaliere et al. (US 3,961,254).

As per claim 34, Hashizume teaches a method of testing a semiconductor integrated circuit, which has internal logical circuitry, a plurality of flip-flops for scan testing said internal logical circuitry and which has

a normal operation mode and a test mode for performing said scan testing (fig. 1A, 1B, 2, col. 5, line 42-col. 6, line 14, col. 6, lines 46-51, col. 7, lines 12-25, Hashizume).

However Hashizume does not explicitly teach the specific use of memory means connected to said plurality of flip-flops, wherein access to said memory means is prohibited during said test mode.

Cavaliere et al. in an analogous art teach an LSI semiconductor device comprising a memory array, including address, data and buffer registers (col. 6, lines 6-8, Cavaliere et al.). Cavaliere et al. also teach inhibiting access between the logic circuitry and the memory array when the device is in a test mode (col. 6, lines 26-28, Cavaliere et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hashizume's patent with the teachings of Cavaliere et al. by including an additional step of using memory means connected to said plurality of flip-flops, wherein access to said memory means is prohibited during said test mode.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to prevent access to data stored in the memory during the test mode so that the data is not corrupted.

13. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashizume (US 6,539,511 B1) as applied to claim 24 above, and further in view of Bae et al. (KR 2001011641 A).

As per claim 30, Hashizume substantially teaches the claimed invention described in claim 24 (as rejected above). Hashizume also teaches the reset control means (col. 8, lines 46-47, Hashizume) and the scan mode signal (col. 3, line 29, Hashizume).

However Hashizume does not explicitly teach the specific use of obtaining an edge detection signal corresponding with the rising edge and the falling edge of the scan mode signal.

Bae et al. in an analogous art teach a rising edge detection unit for detecting the rising edge of a source clock signal, a falling edge detection unit for detecting falling edge of the source clock signal (abstract, Bae et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hashizume's patent with the teachings of Bae et al. by including an additional step of obtaining an edge detection signal corresponding with the rising edge and the falling edge of the scan mode signal. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to reset the circuit using the rising edge and the falling edge of the scan mode signal.

14. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashizume (US 6,539,511 B1) view of Cavaliere et al. (US 3,961,254).

As per claim 31, Hashizume teaches a semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising: a plurality of flip-flops arranged so as to perform scan testing for said internal logical circuitry; switching at a transition time between said test mode and said normal mode and for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal (fig. 1A, 1b, 2, 36, col. 5, line 42 to col. 6, line 14, col. 6, lines 46-51, col. 7, lines 12-25, col. 33, lines 49 to col. 34 line 8, col. 34, lines 31-43, Hashizume).

However Hashizume does not explicitly teach the specific use of memory means connected to said plurality of flip-flops; and access control means for prohibiting access to said memory means during said test mode in accordance with a mode signal

Cavaliere et al. in an analogous art teach that in an LSI semiconductor…logic circuitry (col. 6, lines 6-8, Cavaliere et al.). Cavaliere et al. also teach that means for inhibiting…test mode (col. 6, lines 25-29, Cavaliere et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hashizume's patent with the teachings of Cavaliere et al. by including an additional step of using memory means connected to said plurality of flip-flops; and access control means for prohibiting access to said memory means during said test mode responsive to said mode signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to control access to the memory during the test mode.

15. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashizume (US 6,539,511 B1) as applied to claim 24 above, and further in view of DeLisle et al. (US 5,283,889).

As per claim 35, Hashizume substantially teaches the claimed invention described in claim 24 (as rejected above). Hashizume also teaches the scan chain that is responsive to a rising and falling of the scan mode signal for resetting said plurality of flip-flops (fig. 36, col. 33, lines 54-65, Hashizume).

However Hashizume does not explicitly teach the specific use of a dummy flip-flop.

DeLisle et al. in an analogous art teach that a reset signal...the dummy flip-flop 120 (col. 16, lines 54-58, DeLisle et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hashizume's patent with the teachings of DeLisle et al. by including an additional step of using a dummy flip-flop.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a dummy flip-flop would provide the opportunity to reset the scan flip-flops using the scan mode signal.

16. Claims 36, 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashizume (US 6,539,511 B1) in view of Cavaliere et al. (US 3,961,254).

As per claim 36, Hashizume teaches a semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising: an inputted scan pattern to a scan chain between said scan in terminal and a scan out terminal; a plurality of flip-flops arranged in said scan chain so as to perform scan testing for said internal logical circuitry responsive to said scan pattern; a scan mode input providing a scan mode signal for switching said internal logic circuitry between said normal operation state and a scan operation state including said test mode; and a reset means for resetting said plurality of flip-flops at a transition time, between said test mode and said normal mode, responsive to said scan mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal, wherein said reset means is responsive to a reset signal inputted from a reset input terminal and resets said plurality of flip-flops at said transition time, between said test mode and said normal mode, in accordance with said mode signal (fig. 1A, 1B, 2, 4, 14,

27, 36, col. 5, lines 60-65, col. 6, lines 45-51, lines 56-67, col. 7, lines 39-43, col. 14, line 55 to col. 15, line 6, col. 15, lines 18-23, lines 40-46, col. 23, lines 53-58, col. 24, lines 12-13, col. 33, lines 49 to col. 34 line 8, col. 34, lines 31-43,Hashizume) and further comprising output control means that is connected serially to said plurality of flip-flops, and which outputs data that is supplied during said test mode while prohibiting the outputting of data that is supplied during said normal operation mode (fig. 14, col. 14, lines 55-67, col. 15, lines 11-20, Hashizume).

However Hashizume does not explicitly teach memory means connected to said plurality of flip-flops; and access control means for prohibiting access to said memory means during said test mode responsive to said mode signal.

Cavaliere et al. in an analogous art teach that in an LSI semiconductor…logic circuitry (col. 6, lines 6-8, Cavaliere et al.). Cavaliere et al. also teach that means for inhibiting…test mode (col. 6, lines 25-29, Cavaliere et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hashizume's patent with the teachings of Cavaliere et al. by including an additional step of using memory means connected to said plurality of flip-flops; and access control means for prohibiting access to said memory means during said test mode responsive to said mode signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to control access to the memory during the test mode.

- As per claim 37, Hashizume and Cavaliere et al. teach the additional limitations.

Hashizume teaches that said plurality of flip-flops are arranged so as to perform scan testing for said internal logical circuitry (fig. 1A, 1B, 4, col. 5, lines 52-54, col. 6, lines 3-6, Hashizume).

17. Claims 38, 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashizume (US 6,539,511 B1) and Cavaliere et al. (US 3,961,254) as applied to claim 36 above, and further in view of Tamamura et al. (US 6,118,316).

As per claim 38, Hashizume and Cavaliere et al. substantially teaches the claimed invention described in claim 36 (as rejected above). Hashizume also teaches that the reset means resets said plurality of flip-flops (col. 6, lines 56-67, col. 7, lines 31-33, Hashizume).

However Hashizume and Cavaliere et al. do not explicitly teach the specific use of the transition detection means for detecting the transition time of said logical level of said mode signal.

Tamamura et al. in an analogous art teach that as shown in FIG. 3, the pulse generating circuit 5 detects a transition timing (an edge) of the input data 1b, and generates a detected pulse signal 5a so as to be triggered by the transition timing (fig. 3, col. 1, lines 53-56, Tamamura et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hashizume's patent with the teachings of Tamamura et al. by including an additional step of using the transition detection means for detecting the transition time of said logical level of said mode signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the transition detection means for detecting the transition time of said logical level of said mode signal would provide the opportunity to reset the circuit elements for the new mode of circuit operation.

- As per claim 39, Hashizume, Cavaliere et al. and Tamamura et al. teach the additional limitations.

Hashizume teaches that the reset means resets said plurality of flip-flops (fig. 2, 4, col. 6, lines 56-67, col. 7, lines 31-33, Hashizume).

Tamamura et al. teach transition detection means for detecting the transition time of said logical level of said mode signal (fig. 3, col. 1, lines 53-56, Tamamura et al.).

18. Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashizume (US 6,539,511 B1) and Cavaliere et al. (US 3,961,254) as applied to claim 36 above, and further in view of Bae et al. (KR 2001011641 A).

As per claim 40, Hashizume and Cavaliere et al. substantially teach the claimed invention described in claim 36 (as rejected above). Hashizume also teaches the reset control means (col. 8, lines 46-47, Hashizume) and the scan mode signal (col. 3, line 29, Hashizume).

However Hashizume and Cavaliere et al. do not explicitly teach the specific use of obtaining an edge detection signal corresponding with the rising edge and the falling edge of the scan mode signal.

Bae et al. in an analogous art teach a rising edge detection unit for detecting the rising edge of a source clock signal, a falling edge detection unit for detecting falling edge of the source clock signal (abstract, Bae et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hashizume's patent with the teachings of Bae et al. by including an additional step of obtaining an edge detection signal corresponding with the rising edge and the falling edge of the scan mode signal. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to reset the circuit using the rising edge and the falling edge of the scan mode signal.

19. Claims 41, 43, 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashizume (US 6,539,511 B1) in view of Tamamura et al. (US 6,118,316).

As per claim 41, Hashizume teaches a semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising: a scan path between a scan in source receiving a scan pattern and a scan output with a scan chain including a plurality of scan flip-flops formed between said scan in source and the scan output, said scan flip-flops configured to make scan testing possible according to said scan pattern; a scan mode signal provided for switching said internal logic circuitry between said normal operation mode and said test mode responsive to said scan mode signal; scan operations are inhibited without resetting at the time of initiating scan operations or normal operations without being reset upon termination of scan operations (fig. 1A, 1B, 2, 4, 14, 27, 36, col. 5, lines 60-65, col. 6, lines 45-51, lines 56-67, col. 7, lines 39-43, col. 14, line 55 to col. 15, line 6, col. 15, lines 18-23, lines 40-46, col. 23, lines 53-58, col. 24, lines 12-13, col. 33, lines 49 to col. 34 line 8, col. 34, lines 31-43, Hashizume).

However Hashizume does not explicitly teach a reset input signal for controlling reset of said flip-flops by a reset control block provided to detect transition time of a logical level of the scan mode signal by an

edge detection signal having a pulse length that is at least equal to or greater than one clock period of a system clock.

Tamamura et al. in an analogous art teach that as shown in FIG. 3, the pulse generating circuit 5 detects a transition timing (an edge) of the input data 1b, and generates a detected pulse signal 5a so as to be triggered by the transition timing (fig. 3, col. 1, lines 53-56, Tamamura et al.). The examiner would also like to point out oscillation output signal 3a in fig. 3.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hashizume's patent with the teachings of Tamamura et al. by including an additional step of using a reset input signal for controlling reset of said flip-flops by a reset control block provided to detect transition time of a logical level of the scan mode signal by an edge detection signal having a pulse length that is at least equal to or greater than one clock period of a system clock.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to reset the circuit elements for the new mode of circuit operation.

- As per claim 43, Hashizume and Tamamura et al. teach the additional limitations.

Hashizume teaches that during scan testing, said scan pattern is inputted to the scan flip-flops so that by a shift out of said scan chain, data that is to be checked for scan testing are shifted out from the scan output (fig. 36, col. 33, line 66 to col. 34, line 8, Hashizume).

- As per claim 44, Hashizume and Tamamura et al. teach the additional limitations.

Hashizume teaches that said reset control block includes a pair of flip-flops and logical output circuits arranged (fig. 2, 4, col. 6, lines 56-67, col. 7, lines 31-33, col. 8, lines 40-55, Hashizume).

Tamamura et al. teach to detect transition time of a logical level of the scan mode signal (fig. 3, col. 1, lines 53-56, Tamamura et al.).

20. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashizume (US 6,539,511 B1) and Tamamura et al. (US 6,118,316) as applied to claim 41 above, and further in view of DeLisle et al. (US 5,283,889).

As per claim 42, Hashizume and Tamamura et al. substantially teach the claimed invention described in claim 41 (as rejected above). Hashizume also teaches the scan path (fig. 36, col. 33, lines 54-65, Hashizume).

However Hashizume and Tamamura et al. do not explicitly teach the specific use of a dummy flip-flop.

DeLisle et al. in an analogous art teach that a reset signal...the dummy flip-flop 120 (col. 16, lines 54-58, DeLisle et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hashizume's patent with the teachings of DeLisle et al. by including an additional step of using a dummy flip-flop.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a dummy flip-flop would provide the opportunity to reset the scan flip-flops using the scan mode signal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Patent Examiner